con layers 32A, 32B, each of a thickness, e.g., of about 1 μm., are deposited, with an intervening oxidation step. In the etching step (FIGS. 13C or 18) to form trench 63, the oxide layer 90 (e.g., 1000 angstroms) serves as an etch stop to protect the first polysilicon layer 32A. Layer 32A is N-doped to a resistivity conventionally used in polysilicon contacts. Doping can be done before depositing layer 32B or after removing it, such as the step shown in FIG. 14A. Layer 32A can serve as the gate conductive layer without metallization, although deposition of gate metal after removal of oxide layer 90 is preferred for high speed devices.

Accordingly, one should now see how the method proposed by the invention offers a dramatic improvement over the best-known prior art procedures. Mask-dependent, catastrophic errors or defects in a finally produced semiconductor device are obviated. Doping is precisely and effectively controlled to minimize parasitics. Conductive contacts for both the source and gate can be formed in one step and effectively isolated without separate masks. As a significant consequence, the entire usable area of a silicon wafer can be employed with assurance, even in the manufacture of a single, extremely large device, that it will be free from a mask-dependent failure.

In addition to the advantages discussed above which result from employment of the method of the present invention, there are certain others which are worth noting. By minimizing the number of masking steps required, manufacturing time and the number of required manufacturing personnel are reduced. Also, less expensive processing equipment can be used than is now required. Additionally, by shrinking the overall processing time, this reduces the work-in-process inventory, and, of course, such is an important expense consideration. Employing the technique of the invention in the computer-controlled laser/ion beam applications, one can design and generate a semiconductor device easily in an extremely short period of time.

Yet another advantage offered by the invention is that it eliminates the kind of defects which can result from temperature and humidity changes that can occur in the working environment over the time required to complete multiple masking steps. The mask-surrogate pattern-definers which are created, built into the structure as they are, eliminate these possibilities.

Thus, one should see how the important objects of the invention, and the advantages claimed for it, are readily obtained. The teachings of the invention are not limited to a recessed-source power MOSFET. For example, they can be applied advantageously to a recessed-gate process and structure.

Having described and illustrated the principles of our invention in a preferred embodiment and variations thereof, it should be apparent to those skilled in the art that the invention may be modified in arrangement and detail without departing from such principles. We claim all modifications coming within the scope and spirit of the following claims.

We claim:

1. A method employing no more than one independent mask of producing a plural-functional-region MOS semiconductor device in a substrate structure including a gate oxide layer on an upper surface of a semiconductor substrate, said method comprising:

forming over the oxide layer a dopant protective layer,

creating a mask-surrogate pattern-definer having a defined outline characteristic in such protective layer,

exposing a portion of the upper surface of the substrate within a range bounded by the defined outline characteristic,

performing first and second doping steps in the exposed portion of the upper surface of the substrate to form a first diffusion of a first dopant type extending to a first depth within said region and to a first lateral width determined by the defined outline characteristic and to form a second diffusion of a second dopant type of polarity opposite the first dopant type and extending to a second depth within said region and a second lateral width determined by the defined outline characteristic,

the second depth and width being less than the first depth and width, respectively, so that the second diffusion is contained within the first diffusion,

forming a trench in the exposed upper surface portion of the substrate, the trench having a base and sidewalls in which a lower substrate surface is exposed,

the trench being formed to a trench depth less than the first diffusion depth and greater than the second diffusion depth and a trench width less than the second lateral width, so as to form separate source regions of the second diffusion along opposed sidewalls of the trench and to space the lower substrate surface of the base of the trench below the upper surface of the substrate,

forming a gate conductive layer on the oxide layer and a source conductive layer on the base of the trench in contact with the lower substrate surface,

the gate and source conductive layers each conforming to the defined outline characteristic and being spaced vertically apart by the spacing of the lower substrate surface on which the source conductive layer is deposited below the upper substrate surface portion on which the oxide layer is deposited, and

the source conductive layer and trench sidewalls being mutually formed so that the source conductive layer electrically contacts the source regions along said sidewalls.

2. A method according to claim 1 in which the second diffusion is formed in two separate steps, including introducing the second dopant to the substrate prior to trenching and diffusing the second dopant after trenching.

3. A method according to claim 2 in which introducing the second dopant causes defects in the exposed upper surface portion of the substrate and the trenching substantially reduces said defects and the likelihood of defects occurring in a subsequent diffusion.

4. A method according to claim 1 including a third doping step, following forming the trench, to form a third diffusion of the first dopant type in the substrate in the base of the trench, the third diffusion limiting the extent of downward diffusion of the second dopant type and increasing the conductivity of the first dopant type beneath the trench and second diffusion.

5. A method according to claim 1 in which the second diffusion is formed in separate first and second substeps, including:

a first substep of introducing the second dopant to the substrate prior to trenching;

a third doping step, following forming the trench, to introduce additional dopant of the first type into the substrate in the base of the trench; and